METHODS AND ARRANGEMENTS FOR LINK POWER REDUCTION

ABSTRACT

Methods, and arrangements for extension of clock and data recovery (CDR) loop latency and deactivation of CDR circuits are disclosed. In particular, embodiments address situations in which a receiver, designed to handle spread spectrum clocking, may not always or continuously encounter spread spectrum signals. As a result, power consumption by the receivers may be reduced. Embodiments identify situations in which spread spectrum clocking is unnecessary and may adapt the CDR loop to operate with less power consumption by, e.g., reducing the operating frequency of CDR circuits. For instance, some embodiments employ a flywheel circuit, incorporated into many spread spectrum CDR loops to accelerate adjustments to a sampling clock, to determine when spread spectrum signals are not being encountered. A loop latency controller may then, advantageously, reduce power consumption by reducing frequencies of operation and voltages, and merging or simplifying stages.